APPLICATION NOTE 318

Ericsson Power Modules

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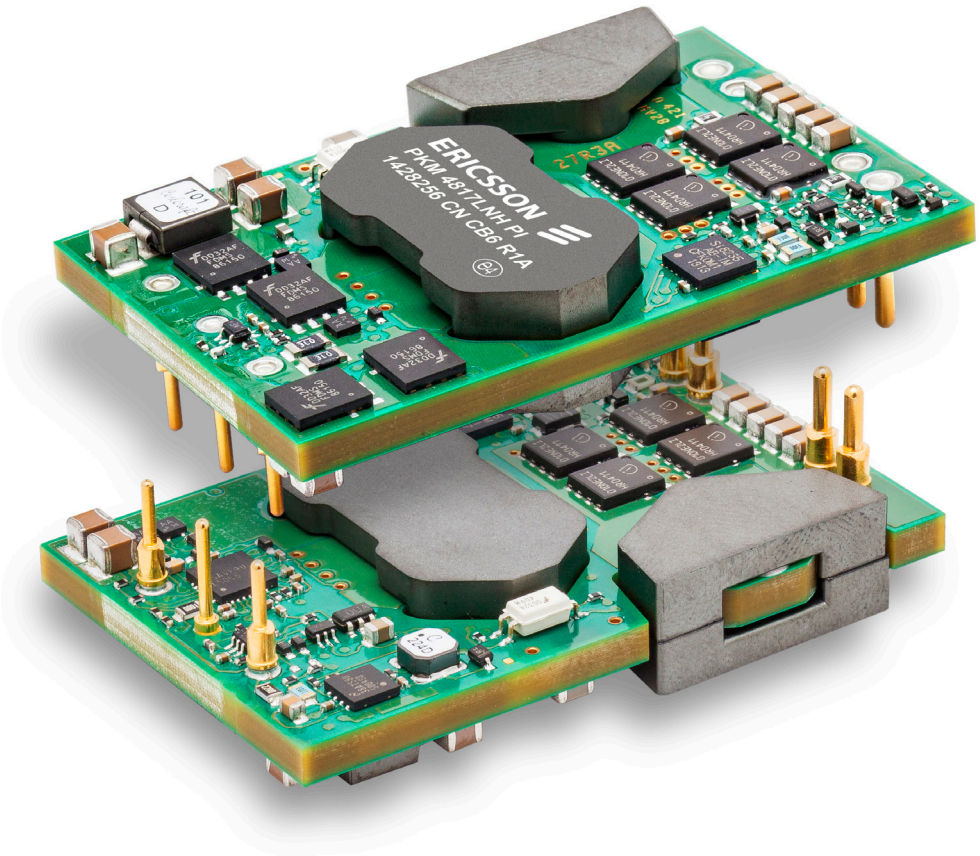

PKM 4817LNH PARALLEL OPERATION WITH DROOP LOAD SHARING

ABSTRACT

The PKM 4817LNH offers passive load sharing allowing multiple products to be connected in parallel. This feature is typically used to increase power output on the same rail, providing redundancy against a product failure, or distribute thermal heat over a larger board area. Paralleling may also aid in streamlining your Bill of Materials by replacing the need for separate products with higher power requirements.

INTRODUCTION

This Application Note describes the parallel operation and load sharing of the product in greater detail. It also describes the design considerations to be made in order to optimize the current sharing for maximum output power.

For definitions and specifications see the Technical Specification for PKM 4817LNH.

CONTENTS

PASSIVE CURRENT SHARING

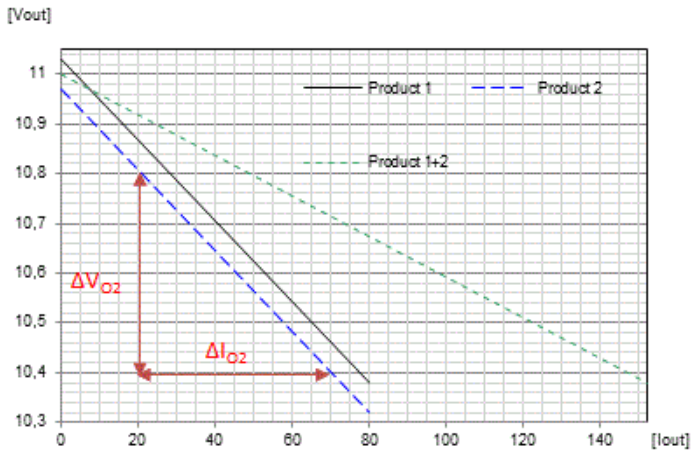

Figure 1 Typical output current from two products with 60mV output voltage initial setting tolerances but with equal output resistance.

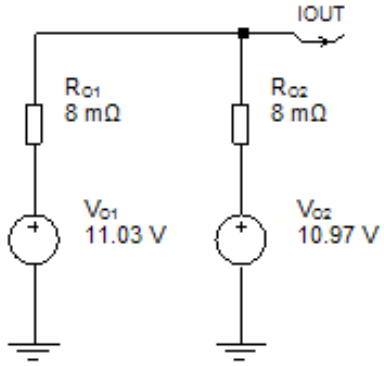

Figure 2 A simplified schematic model of two paralleled PKM 4817LNH.

Passive current sharing is achieved by having a droop load share, i.e. the output voltage of the product will decrease when the load current is increased, see Figure 1. This can also be expressed as an output resistance of the product, see schematic representation in Figure 2.

In the example above both products have the same output resistance, $R_O = R_{O1} = R_{O2}$, since the slopes are constant and parallel. R_O can be estimated directly from Figure 1 by using product 2 as shown in Equation 1:

$$R_0 = \frac{\Delta V_0}{\Delta I_0} \approx \frac{10.8 - 10.4}{70 - 20} = 0.4/50 = 8m\Omega$$

Equation 1

Note that when the products are connected in parallel they will share the same output voltage. Only the output current will differ. E.g. from Figure 1 at 10.8 V, product 1 delivers 28 A and product 2 delivers 20 A, approximately.

Difference in output voltage initial setting (Vo at 0 A), output resistance and difference in output resistance are the parameters that defines the current sharing accuracy. The long term drift is negligible for PKM 4817LNH.

If the droop is very low the products will not share current well due to different initial voltage setting. A too high droop on the other hand will make current sharing well but limit the available output power. The droop is chosen such that the available output power for parallel products is optimized.

Since the output currents of paralleled products are not identical one of the products will reach max current before the other, therefore the expected total output current is less than twice the output current of a single product. In practice the maximum output current could also be limited by the maximum allowed operating temperature of the warmest product.

The PKM 4817LNH product is verified with up to three parallel products; however, theoretically there is no upper limit in the number of paralleled products.

COOLING

Due to the small form factor and high output power, it is important that the products have adequate cooling to be able to deliver high output currents. Figure 3 below shows typical power dissipation vs output current for a single product.

The power dissipation will make the product warmer, how much warmer depends on the thermal resistance Rth, found in the technical specification. Rth is a function of air velocity. Rth is also dependent on whether the product is open frame, base plate or supported with heat sink.

The product also uses its pins for cooling by transferring heat to the mother board. For efficient heat transfer, it is recommended that the pins are connected to copper planes in the mother board. The estimated internal temperature at point P1 of the product can be calculated using Equation 2:

$$T_{P1} = T_{amb} + R_{th} * P_d$$

Equation 2

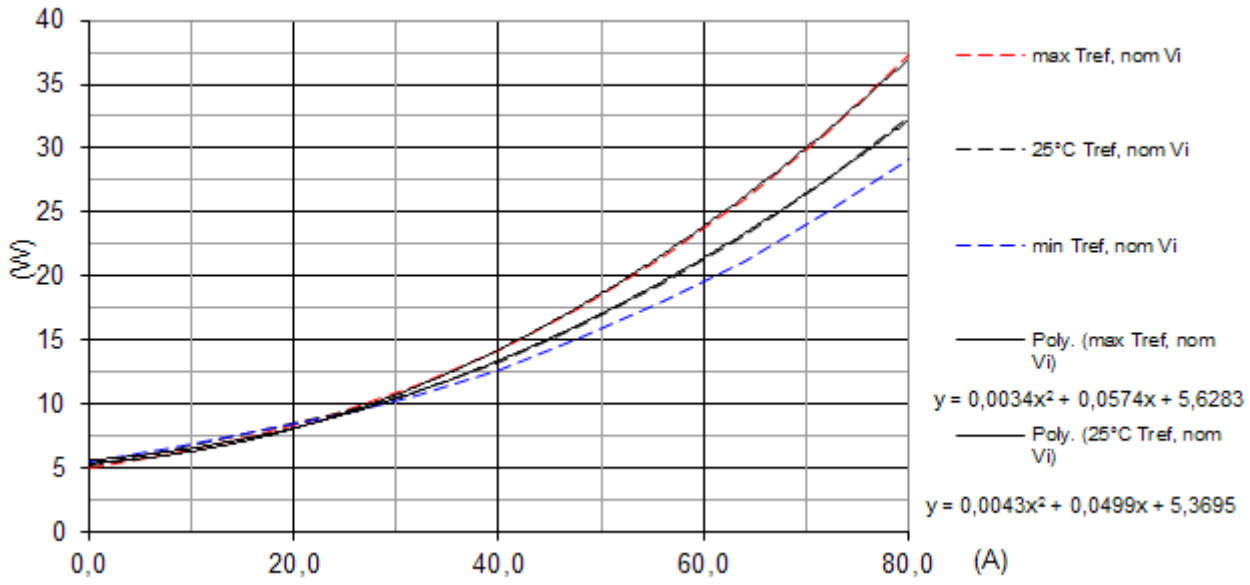

Figure 3 Measured Power Dissipation, P_d vs output current for TP1= -30, 25 and 90°C.

OPERATION

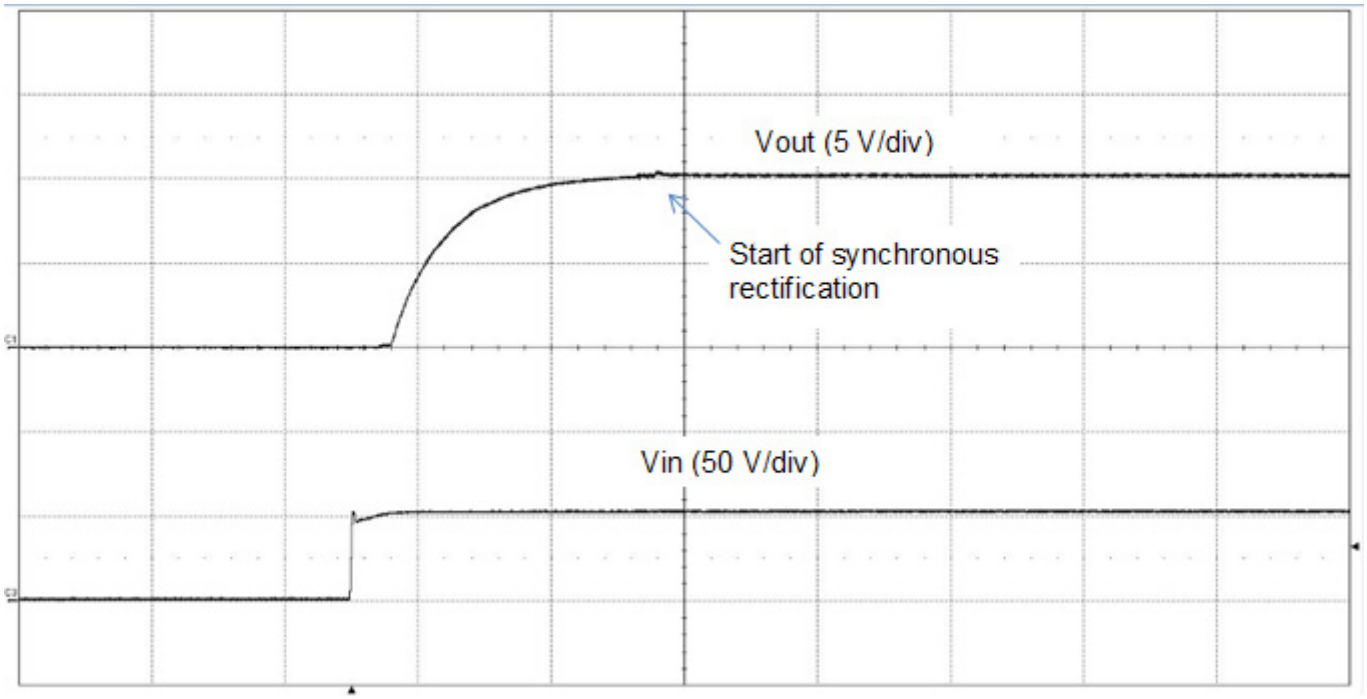

Figure 4 Start-up for two parallel products with 152 A resistive load and Cout = 10 mF. (5 ms/div).

Turn-On

It can take about 20 ms after a start-up before good current sharing is established. During the entire ramp-up time, diode rectification is enabled (i.e. synchronous rectification FETs are all off), as shown in Figure 4. This is to avoid dips in output voltage and high reverse currents when starting one product in an array of paralleled products. It is recommended to limit the load current during this initial 20 ms to between the single product rating and the paralleled products rating.

The maximum load at start-up is also affected by output capacitance. Since the output voltage ramp-up is typically 4.5 ms the current into the external capacitor during ramp-up can be calculated as in Equation 3:

$$I_{Cout} = C_{OUT}\frac{\Delta V_{OUT}}{\Delta t} \approx C_{OUT}\frac{10V}{4.5ms}$$

Equation 3

where 10 V is the approximate ΔV_{OUT} from Figure 4.

With an output capacitance of 10 mF, the current into the output capacitance during ramp-up is 22 A. So the maximum available output load current during start-up will be reduced by 22 A. The ramp-up time can be as low as 2 ms at V_I=60 V.

Start-up of parallel products, with slow slew rate on the input voltage, can cause one product to start before the other, due to different turn-on voltage. The available output current during the time of single product operation will then be reduced to the single product rating.

Turn-off and Input Voltage between 45 and 51 V

In this region and when the product is turned off with V_I the product will be in regulated ratio mode (output voltage is proportional to input voltage). In this mode it is important that paralleled products share the same input voltage, otherwise the product with the lowest input voltage will give the lowest output voltage and clamp the other product to this lower output voltage.

DESIGN CONSIDERATIONS

Layout Considerations

Connect the outputs together as close to the load as possible. Never connect diodes or other current blocking devices between the inputs of paralleled products and keep the resistance and inductance between the inputs as low as possible.

If the output current of each product is higher than 50 A, the double pin version of the product is recommended. The product also uses its pins for cooling by transferring heat to the mother board. For efficient heat transfer, it is recommended that the pins are connected to copper planes in the mother board.

Input Capacitance

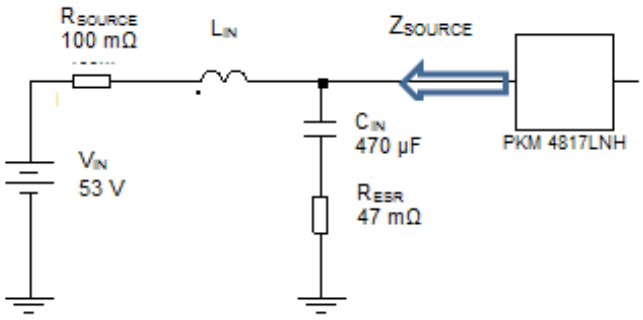

Figure 5 Source impedance and external input capacitance.

The recommended input capacitance, C_{IN}, is 470 µF or higher (of low ESR type) and it should be placed close to the input of each product. Note that the ESR of electrolytic capacitors increase at cold environment.

If an external input filter is used, the recommended peak source impedance Z_{source_peak}, is below 2 Ω per product. Otherwise input oscillations may occur at start-up, or at a high output current transients.

The source resistance, R_{source} should be less than 100 mΩ/product to avoid the under voltage lockout to be activated. I.e. for two parallel products R_{source} should be less than 50 mΩ and Z_{source_peak} should be below 1 Ω.

Output Capacitance for Parallel Products

The output capacitors of ceramic type should be placed close to the load for efficient decoupling and also to reduce the Q-value of the output filter. Ceramic type of output capacitors has a very low ESR value (e.g. a single 47 µF, 1210, 16 V has an ESR of about 3 mΩ), normally resulting in a high Q-value of the output filter. The Q-value can be damped by using bulk capacitors with higher ESR values in parallel with the ceramic type.

BEAT FREQUENCY

When paralleling PKM 4817LNH products, a beat frequency can be noticed on the output, as illustrated in Figure 6a. This is due to slightly different switching frequencies between the products.

If the beat frequency is a problem, an external 10 nF Y-capacitor can help to reduce it. Since this is a low frequency phenomenon the placement of the Y-capacitor is not critical.

See example of appropriate placement of the Y-capacitor connected across the isolation barrier in Figure 7.

In Figure 6b the output from a single product is shown for comparison.

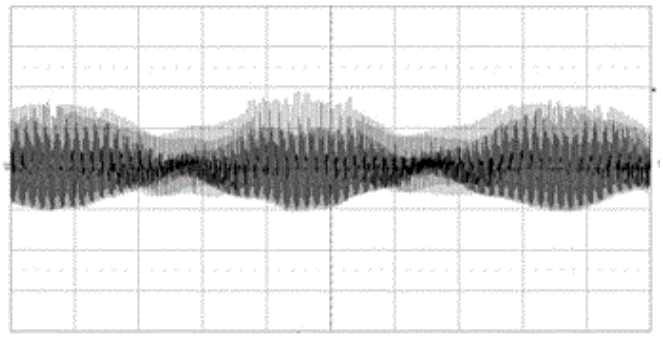

Figure 6a Output ripple, two parallel products 100 us/div, 20 mV/div.

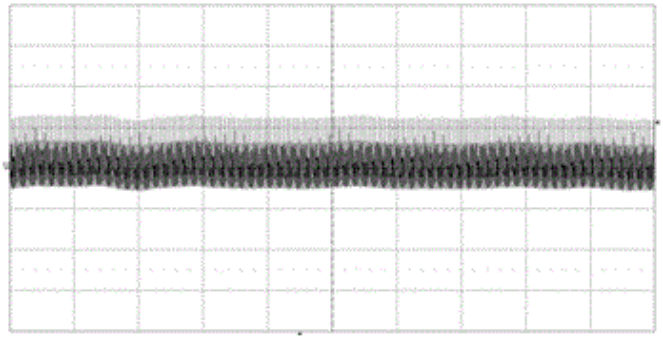

Figure 6b Output ripple single product 100 us/div, 20 mV/div.

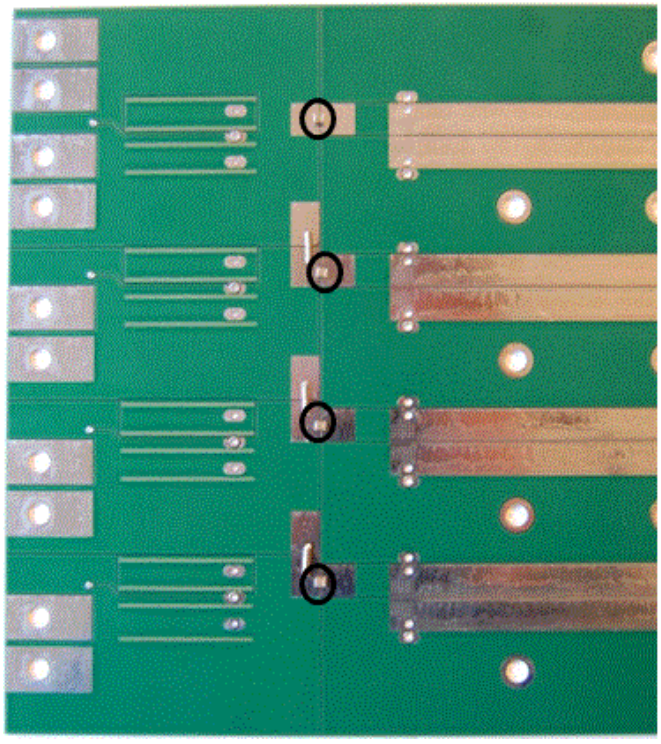

Figure 7 A PKM-NH Reference board, TVA 170 41, Test board for up to four parallel PKM 4817LNH, showing Y-capacitor locations on the backside of the board.

PARALLEL PRODUCTS CURRENT UNBALANCE

A statistical model has been built using measured data of Ro and Vo from two production lots. This model assumes a thermal resistance of 1.4 K/W for each product and an ambient temperature of 40°C. This gives a TP1 temperature of about 90°C, see Equation 2.

Ro is defined with temperature dependence as a 3-sigma gauss distribution with tolerance 3.3 %. (8 ±0.26 mΩ) at 25°C, α=3.9m K^{-1}).

Vo at 0 A is defined as a 3-sigma Gauss distribution with tolerance 0.6 % (11 V ±66 mV).

Simulation Results (Simetrix)

The output current difference, I_{diff}, between two products was simulated in Simetrix using the Monte Carlo method including 1000 runs. I_{diff} is shown as a histogram[1] in Figure 8. I_{diff} has been divided in 15 "bins" of approximately 1 A width. Within each bin the number of paralleled pairs is plotted on the y-axis. This gives a rough sense of the I_{diff} distribution. It was found that I_{diff} is Gaussian distributed with a standard deviation of 2.5 A.

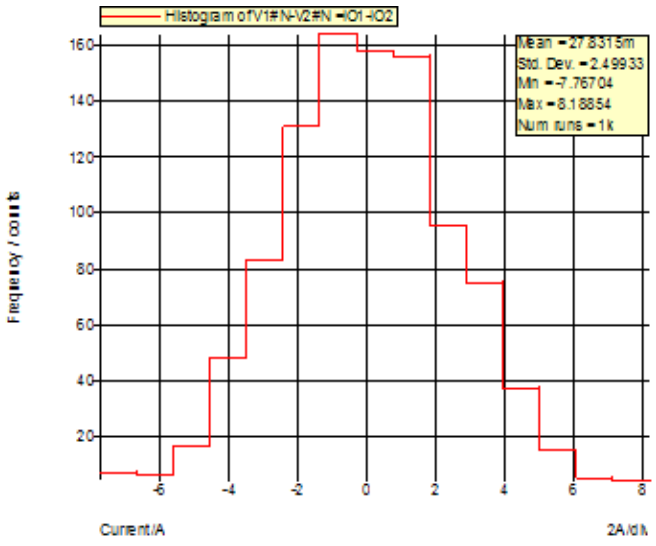

Figure 8 Monte Carlo 1 k runs. Histogram of statistical output current difference (on x-axis) at a total output current of 160 A. TP1 is around 90°C.

Figure 9 shows the probability function of $|I_{diff}| \geq x$, Io=160 A, TP1 = 90°C.

From Figure 10, product 2 has an output voltage of 10.32 V at 80 A. At 10.32 V product 1 delivers 68 A so the worst case current difference is 12 A.

From Figure 9 we can see that the probability of this to happen is around 1.5 ppm. The corresponding predicted temperatures at P1 are 92 and 80°C.

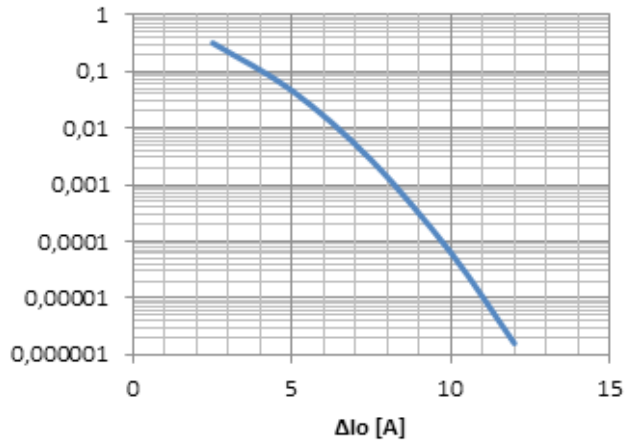

Figure 9 Probability function of $|I_{diff}| \geq x$. TP1 is around 90°C.

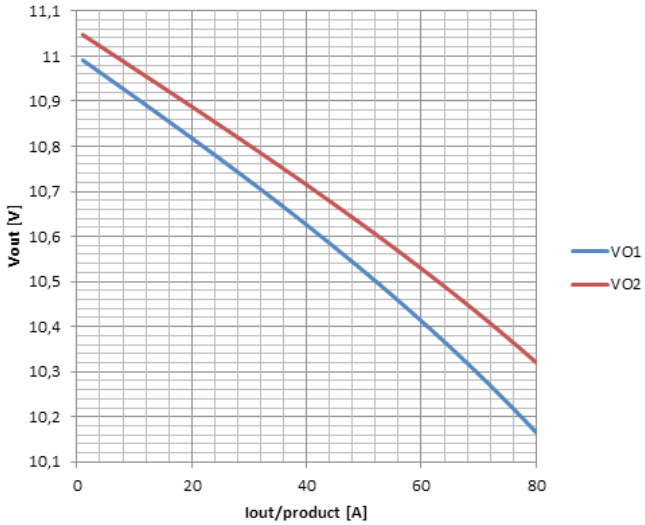

Figure 10 Predicted worst case current share with 4.5 σ output voltage difference at 0 A and +3 σ on RO1 and -3 σ on RO2. Rth=1.4 K/W. Ambient temperature is 40°C for both products. Vin ≥ 51.

1 To construct a histogram, the first step is to "bin" the range of values - that is, divide the entire range of values into a series of small intervals - and then count how many values fall into each interval. A rectangle is drawn with height proportional to the count and width equal to the bin size.

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Formed in the late seventies, Ericsson Power Modules is a division of Ericsson AB that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage products such as point-of-load units ranging in output power from 1 W to 700 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

Power Modules – Americas
Telephone: +1-972-583-5254
+1-972-583-6910

Power Modules – Asia/Pacific
Telephone: +852-2590-2453

Ericsson AB, Power Modules
SE-164 80 Stockholm, Sweden
Telephone: +46 10 716 9620

Power Modules – Japan
Telephone: +81 80 3363 67

Ericsson AB, Power Modules
SE-164 80 Stockholm, Sweden
Telephone +46 10 716 9620
www.ericsson.com/powermodules

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