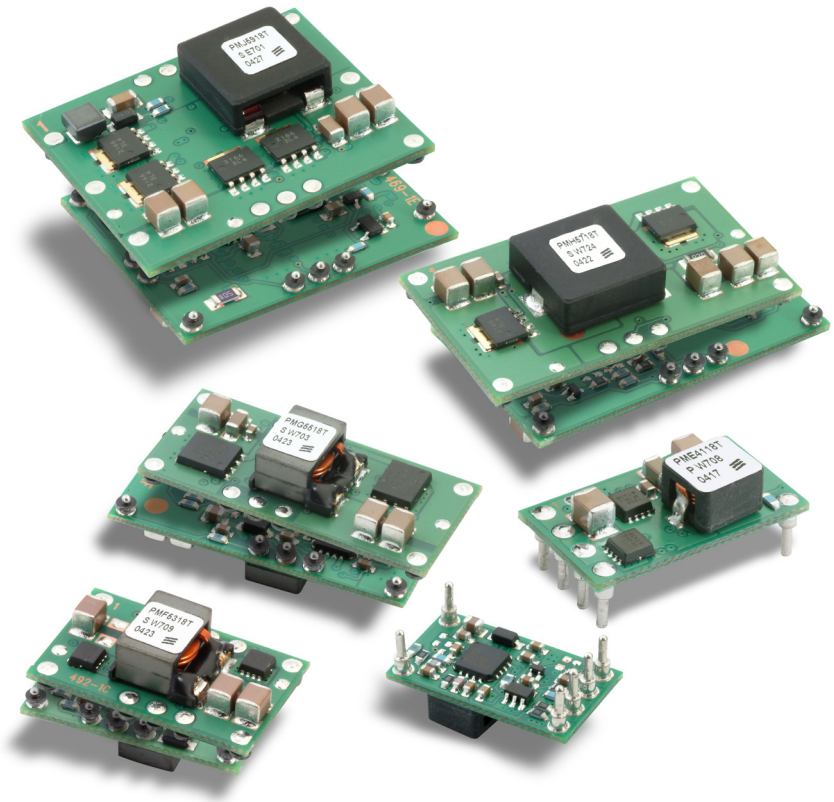
ERICSSON

APPLICATION NOTE 205

Ericsson Power Modules



BASIC FEATURE OF POLA COMPATIBLE POL DC/DC REGULATORS

Abstract

The POLA (point-of-load-alliance) standard products ensure compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA compatible product families of non-isolated, wide output adjust POL (point of load) DC/DC regulators from Ericsson are optimized for applications that require a flexible, small size product with high performance. The operating features of Ericsson's POLA compatible products are described in each product's technical specification. This application note gives a more detailed description of some of these features. Included are the PMD (3/2.25 A), PME (6 A), PMF (10 A), PMG (15/12 A), PMH (22/18 A), PMJ (30/26 A), PMM (60/50 A), PMN (30 A), PMP (16 A) and PMR (50/40 A) product families.

Series	Input Bus	I_{out}	Operating Features							
			On/off Inhibit	Adjust (trim)	OCP	OTP	Auto-Track ™	Margin Up/ Down	Remote Sense	Pre-Bias Startup
PMD	3.0-5.5 V	3 A	x	x	x	x	x			
	4.5-14 V	2.25 A	x	x	x	x	x			
PME	3.3 V/5.0 V	6 A	x	x	x		x			x
	12 V	6 A	x	x	x		x			
PMF	3.3 V/5.0 V	10 A	x	x	x		x	x	x	x
	12 V	10 A	x	x	x		x	x	x	
PMG	3.3 V/5.0 V	15 A	x	x	x		x	x	x	x
	12 V	12 A	x	x	x		x	x	x	
PMH	3.3 V/5.0 V	22 A	x	x	x	x	x	x	x	x
	12 V	18 A	x	x	x	x	x	x	x	
PMJ	3.3 V/5.0 V	30 A	x	x	x	x	x	x	x	x
	12 V	26 A	x	x	x	x	x	x	x	x
PMM	2.95-5.5 V	60 A	x	x	x	x	x	x	x	x
	8-14 V	50 A	x	x	x	x	x	x	x	x
PMN	4.5-5.5 V	30 A	x	x	x	x	x		x	x
	5.5-14 V	30 A	x	x	x	x	x		x	x
PMP	4.5-14 V	16 A	x	x	x	x	x		x	x
PMR	4.5-14 V	50 A	x	x	x	x	x		x	x
	8-14 V	40 A	x	x	x	x	x		x	x

Table 1. Operating Features by series and input bus voltage

Note: DDR versions of the PME, PMF and PMG product families are not included here.

On/Off Inhibit

For applications requiring output voltage on/off control, each family of the PME--PMR products incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage to be turned off.

Figure 1 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pull-up to V_{in} potential. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

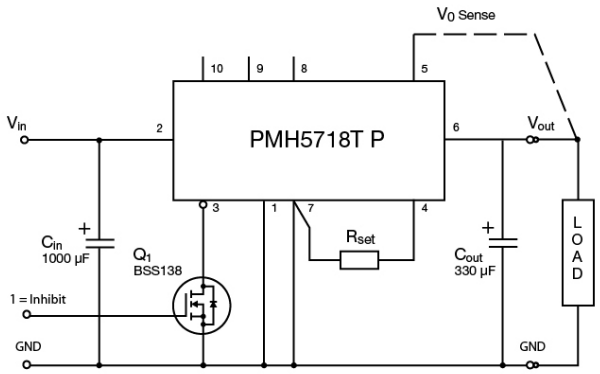


Figure 1. Inhibit function

Turning Q1 on applies a low voltage to the Inhibit control and disables the output of the product. When Q1 is turned off, the product will execute a soft-start power-up. A regulated output voltage is established within about 20 ms.

Adjusting the Output Voltage

The adjustment range of the products (except PMM series which is described in separate section) is from 0.8 V to 2.5 V (3.3 V_{in}), 0.8 V to 3.6 (5.0 V_{in}), and 1.2 V to 5.5 V/ 0.8 V to 1.8 V (12 V_{in}). For an output voltage other than 0.8 V or 1.2 V, a single external resistor, R_{set}, must be connected between the V_0 Adjust and GND pins. Use a 0.1 W resistor. The tolerance should be 1 %, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the POL regulator as possible. Connect the resistor directly between the V_0 Adjust and GND pins using dedicated PCB traces.

Table 2, Table 3 and Table 4 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can be calculated using the following formula:

$$R_{set} = 10\ k\Omega \bullet 0.8\ V / (V_{out} - V_{min}) - Rs\ k\Omega$$

For 3.3 V_{in} bus products: V_{min} = 0.8 V; Rs = 2.49 kΩ
For 5.0 V_{in} bus products: V_{min} = 0.8 V; Rs = 2.49 kΩ
For 12 V_{in} bus products: V_{min} = 0.8 V; Rs = 7.87 kΩ

For PME--PMJ,
PMN--PML 8XXXL: V_{min} = 1.2 V; Rs = 1.82 kΩ

V_{out}	R_{set} (preferred)	V_{out} (actual)
3.3 V	698 Ω	3.309 V
2.5 V	2.21 kΩ	2.502 V
2 V	4.12 kΩ	2.010 V
1.8 V	5.49 kΩ	1.803 V
1.5 V	8.87 kΩ	1.504 V
1.2 V	17.4 kΩ	1.202 V
1 V	36.5 kΩ	1.005 V
0.8 V	Open	0.800 V

Table 2. Preferred values of R_{set} for standard output voltages (3.3/5.0 V_{in})

PME--PMJ, PMN--PMR 8XXXL		
V_{out}	R_{set} (preferred)	V_{out} (actual)
5 V	280 Ω	5.009 V
3.3 V	2.0 kΩ	3.294 V
2.5 V	4.32 kΩ	2.503 V
2 V	8.06 kΩ	2.010 V
1.8 V	11.5 kΩ	1.801 V
1.5 V	24.3 kΩ	1.506 V
1.2 V	Open	1.200 V

Table 3. Preferred values of R_{set} for standard output voltages (12 V_{in})

PME--PMJ, PMN--PMR 8XXXT		
V_{out}	R_{set} (preferred)	V_{out} (actual)
1.8 V	130 Ω	1.800 V
1.5 V	3.57 kΩ	1.499 V
1.2 V	12.1 kΩ	1.201 V
1.1 V	18.7 kΩ	1.101 V
1 V	32.4 kΩ	0.999 V
0.9 V	71.5 kΩ	0.901 V
0.8 V	Open	0.800 V

Table 4. Preferred values of R_{set} for standard output voltages (12 V_{in})

Figure 2 shows the placement of the required resistor.

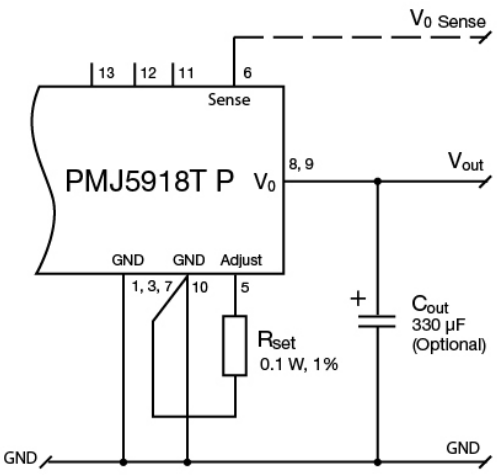


Figure 2. V_0 adjust resistor placement

PMM series

The adjustment range is from 0.8 V to 5.5 V. The adjustment method requires the addition of a single external resistor, RSET, that must be connected directly between the V_0 Adjust and GND pins. Table 5 and Table 6 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages, the value of the required resistor can be calculated.

For PMM 8XXXT using the following formula:
$R_{set} = 10\ k\Omega \bullet 0.8\ V / (V_{out} - 0.8\ V) - 1.696\ k\Omega$

For PMM 4XXXT using the following formula:
$R_{set} = 10\ k\Omega \bullet 0.8\ V / (V_{out} - 0.8\ V) - 2.49\ k\Omega$

PMM 8XXXT		
V_{out}	R_{set} (preferred)	V_{out} (actual)
5.0 V	0.210 kΩ	5.002 V
3.3 V	1.50 kΩ	3.303 V
2.5 V	3.01 kΩ	2.50 V
2.0 V	4.99 kΩ	1.997 V
1.8 V	6.34 kΩ	1.796 V
1.5 V	9.76 kΩ	1.498 V
1.2 V	18.2 kΩ	1.202 V
1.0 V	38.3 kΩ	1.0 V
0.8 V	Open	0.8 V

Table 5. Preferred values of R_{set} for standard output voltages (12 V_{in})

PMM 4XXXT		
V_{out}	R_{set} (preferred)	V_{out} (actual)
2.5 V	2.21 Ω	2.502 V
1.8 V	5.49 kΩ	1.803 V
1.5 V	8.87 kΩ	1.504 V
1.2 V	17.4 kΩ	1.202 V
1.0 V	36.5 kΩ	1.005 V
0.8 V	Open	0.8 V

Table 6. Preferred values of R_{set} for standard output voltages (3.3/5.0 V_{in})

Over-Temperature Protection

The PMH and PMJ product families have over-temperature protection, OTP. These products have an on-board temperature sensor to protect the internal circuitry from excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the Inhibit control is automatically pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases about 10°C below the trip point.

Note: The over-temperature protection prevent excessive thermal stress to the POL regulator. Operation at or close to the OTP threshold is not recommended and can reduce the long-term reliability of the product. Always operate the POL regulator within the specified Safe Operating Area (SOA) for conditions of ambient temperature and airflow.

Auto-Track™ Function

The Auto-Track feature allows for sequencing of multiple PME--PMR. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_{in} see Figure 3.

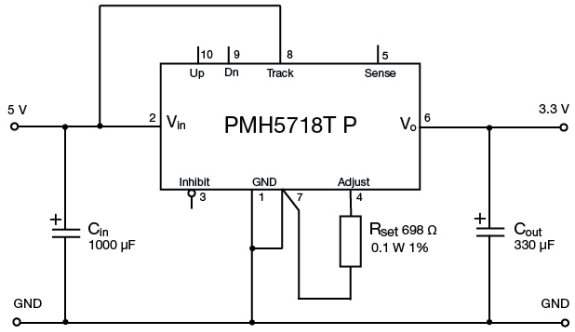


Figure 3. Track pin connection

When the Track pin is connected to the input voltage the Auto-Track function is disengaged. This allows the product to power up entirely under the control of its internal soft-start circuitry. When power-up is under soft-start control, the output voltage will rise at a quicker and more linear rate after input power is applied. Auto-Track works by forcing the output voltage to follow a voltage presented at the Track control pin. This control range between 0 V and the set-point voltage. The Track pin voltage must be allowed to rise above the POL regulators set-point voltage before the POL regulator can regulate at its adjusted set-point voltage.

As an example, if the Track pin of a 2.5 V POL regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

The Auto-Track function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.

The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit. The absolute maximum voltage that may be applied to the Track pin is V_{in}.

For convenience the Track control incorporates an internal RC charge circuit. This operates off the POL regulator input voltage to provide a suitable ramp waveform.

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant products. Connecting the Track control pins of two or more products forces the Track control of all them to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q1 in Figure 4.

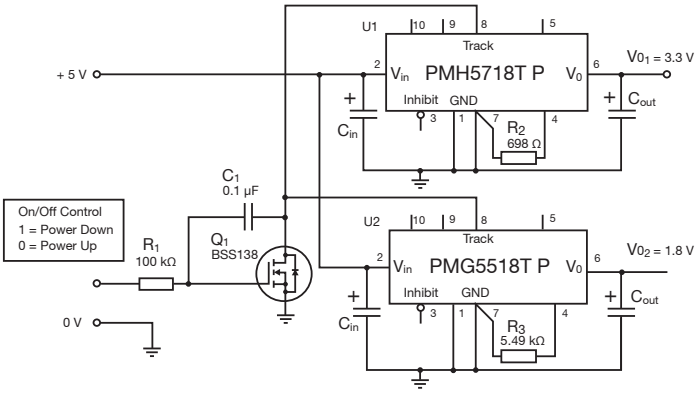


Figure 4. Sequenced power up and power down using Auto-Track

To initiate a power-up sequence the Track control must first be pulled to ground potential. The POL regulator will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the POL regulator has sensed a valid voltage at its input. During this period, it is recommended that the Track pin be held at ground potential.

Applying a logic-level high signal to the circuit's On/Off Control turns Q1 on and applies a ground signal to the Track control. After completing their internal soft-start initialization, the output of all POL regulators will remain at zero volts while Q1 is on. 10 ms after a valid input voltage has been applied to all POL regulators, Q1 can be turned off. This allows the track control voltage to automatically rise toward to the products input voltage. During this period the output voltage of each POL regulator will rise in unison, to its respective set-point voltage.

Figure 5 shows the output voltage waveforms from the circuit of Figure 4 after the On/Off Control is set from a high to a low-level voltage. The waveforms, V_{01} and V_{02} represent the output voltages from the two POL regulators, U1 (3.3 V) and U2 (1.8 V) respectively. V_{01} and V_{02} are shown rising together to produce the desired simultaneous power-up characteristic.

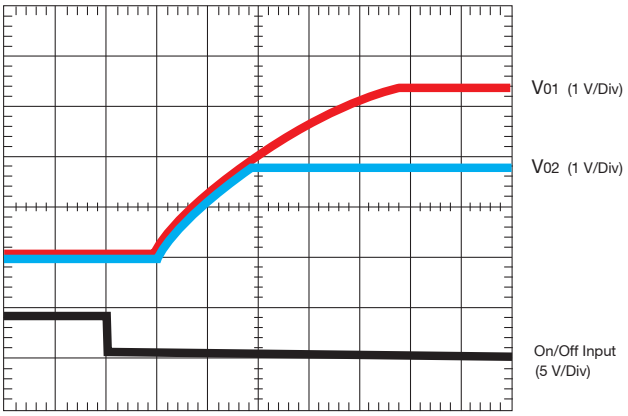


Figure 5. Simultaneous power-up with Auto-Track control

The same circuit also provides a power-down sequence. Power-down is the reverse of power-up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power-down is completed. It also requires Q1 to be turned off relatively slowly, in order to keep Track control voltage within the Auto-track slew rate, 1 V/ms. R_1 and C_1 in Figure 4 limit the pull down rate of the Track control voltage. The values of 100 kΩ and 0.1 µF correlate to a decay rate of about 0.17 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 6 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each POL regulator, the output voltage of each product will decay in unison under Auto-Track control.

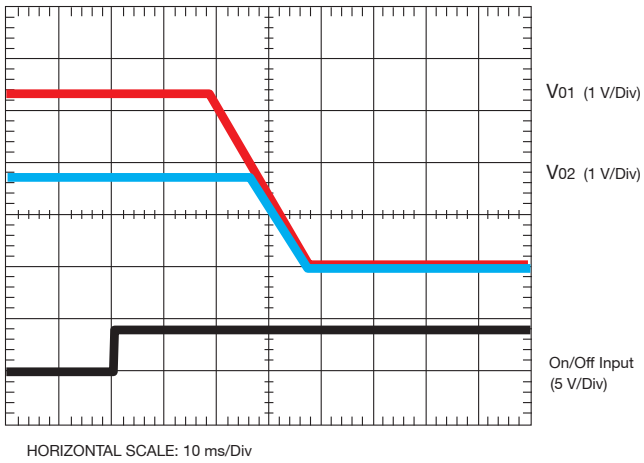


Figure 6. Simultaneous power-down with Auto-Track control

The POL regulator is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore startup into an output pre-bias is not supported during Auto-Track control.

A pre-bias hold off is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.

Pre-Bias Startup Capability

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a POL regulator prior to its output becoming active. This often occurs in complex digital systems when current from another power source is back fed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A pre-bias condition can cause problems with POL regulator that incorporate synchronous rectifiers. This is because under most operating conditions, these types of products can sink as well as source output current.

The products which support pre-bias startup capability will not sink current during startup, or whenever the Inhibit pin is held low. Startup includes the short delay (approx. 10 ms) prior to the output voltage rising, followed by the rise of the output voltage during the internal soft-start control of the POL regulators. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the Track pin, whichever is lowest.

To ensure that the POL regulator does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin); the input voltage must always be greater than the output voltage throughout the power-up and power-down sequence.

Figure 7 shows an application demonstrating the pre-bias startup capability. The startup waveforms are shown in Figure 8. Note that the output current from the POL regulator (I_o) shows negligible current until its output voltage rises above that back fed through diodes D_1 and D_2.

Note: The pre-bias start-up feature is not compatible with Auto-Track. When the POL regulator is under Auto-Track control, it will sink current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off, one of two approaches must be followed when input power is applied to the product. The Auto-Track function must either be disabled or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.

The Auto-Track function can be disabled at power-up by immediately applying a voltage, that is greater than its set-point voltage, to the Track pin of the POL regulator. This can be easily accomplished by connecting the Track pin to V_{in}.

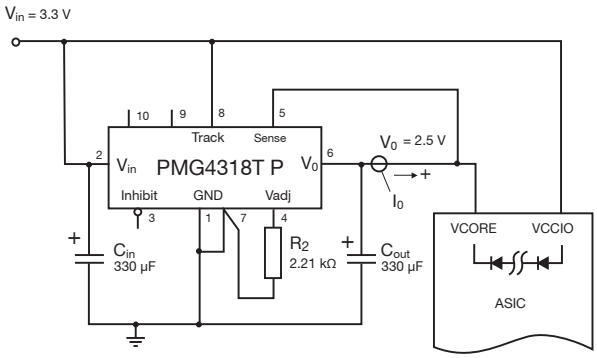


Figure 7. Application circuit demonstrating pre-bias startup

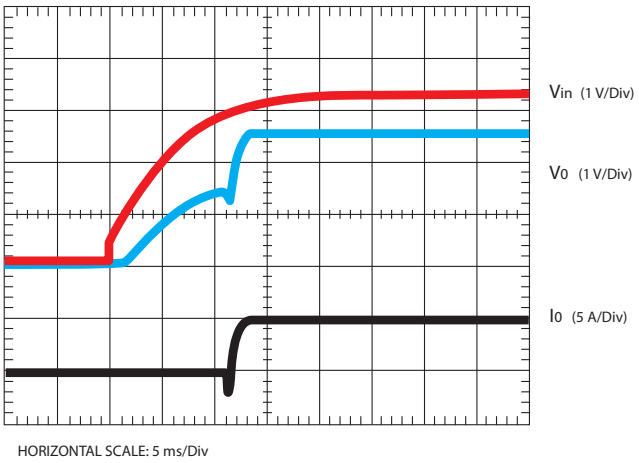


Figure 8. Pre-bias startup waveforms

Ericsson is shaping the future of Mobile and Broadband Internet communications through its continuous technology leadership.

Providing innovative solutions in more than 180 countries, Ericsson is helping to create the most powerful communication companies in the world.

Formed in the late seventies, Ericsson Power Modules is a division of Ericsson AB that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage products such as point-of-load units ranging in output power from 1 W to 800 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

Ericsson AB, Power Modules
SE-164 80 Stockholm, Sweden
Telephone: +46 10 716 9620

Power Modules – Americas
Telephone: +1-972-583-5254
+1-972-583-6910

Power Modules – Asia/Pacific
Telephone: +852-2590-2453

Power Modules – Japan
Telephone: +81 80 3363 67

Ericsson AB, Power Modules
SE-164 80 Stockholm, Sweden
Telephone +46 10 716 9620
www.ericsson.com/powermodules

APPLICATION NOTE
EN/LZT 146 222 R1D