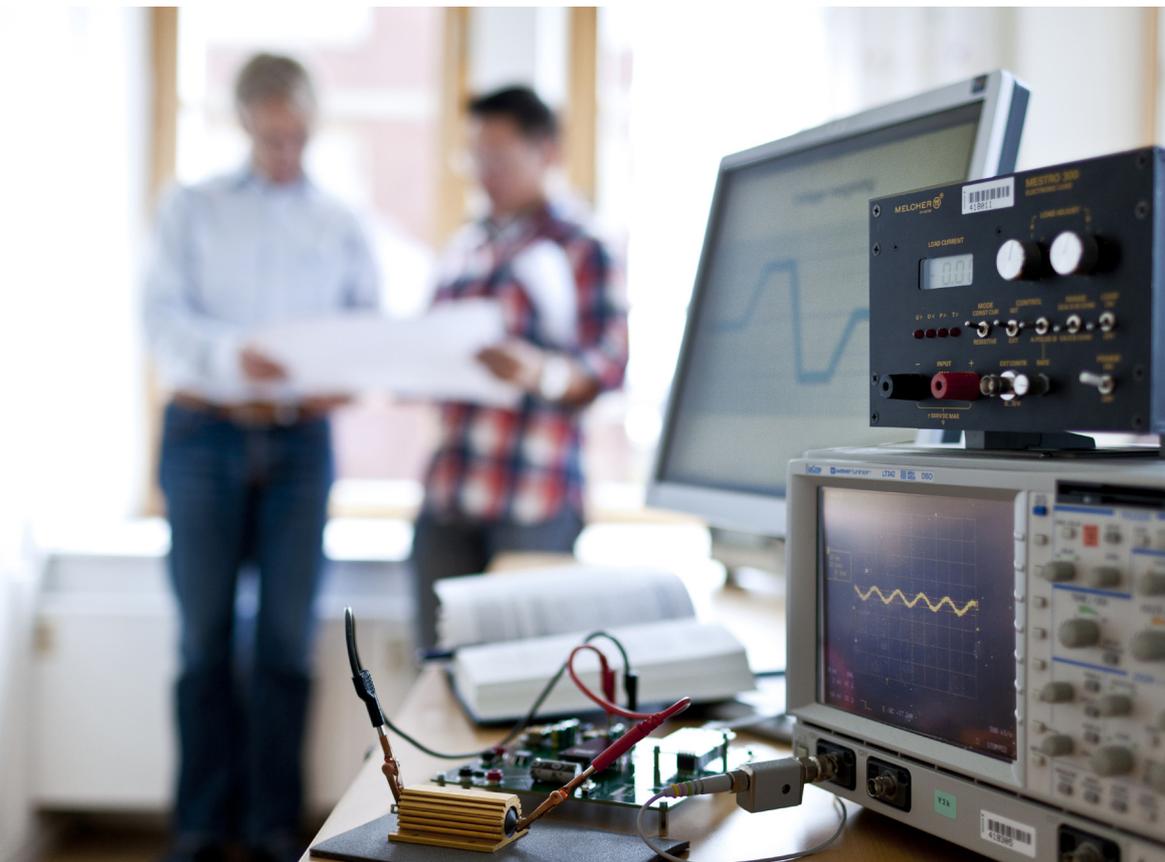




SELECTION OF ARCHITECTURE FOR SYSTEMS USING BUS CONVERTERS AND POL CONVERTERS



DESIGN NOTE 023

Ericsson Power Modules

ericsson.com

Abstract

Most telecom and datacom systems now contain integrated high performance processors, ASICs and FPGAs. These systems are characterized by high levels of current demand at multiple low supply voltages, tight regulation requirements, large and fast dynamic currents. This environment leads to the utilization of some type of distributed power architecture (DPA) to supply operating voltages to these circuits rather than using centralized power architecture. With DPA, the power converters are located in physical proximity to the load circuitry, minimizing DC distribution losses and reducing distribution inductance for enhanced dynamic response performance.

For several years DPA implied a collection of two or more isolated DC/DC converters each supplying one to three output voltages and operating from a common intermediate bus voltage, usually 24 or 48 Vdc. Recently, non-isolated point-of-load (POL) converters have seen more widespread usage. These POL converters are designed to operate from a lower input voltage, usually between 3 and 15 volts and offer fast dynamic response. They are often used in conjunction with an isolated unregulated intermediate bus converter (IBC) that is employed to supply the input voltage for the POL converters at a voltage level that allows for their efficient operation. POL converters can also be used in conjunction with a conventional isolated and regulated DC/DC converter. System designers are often conflicted about which of these two architectures (unregulated bus converter or regulated bus converter) to use in any given application. Efficiency, dynamic response, circuit board area and cost are often the primary criteria to be optimized. The purpose of this design note is to describe the characteristics of the two approaches and to provide comparisons between the two that will be helpful for power system architects when making this design/decision.

Description of Regulated Bus Implementation

A typical power system configured with a regulated bus approach is shown in Figure 1. This system requires four operating voltages, 3.3, 1.8, 1.5 and 1.2 volts. The highest power and current demand is on the 3.3V supply rail. The system shown here is a conventional DPA system with an isolated DC/DC converter operating from the -48V telecom bus and supplying the required regulated 3.3V current to the load circuitry. The DC/DC converter output current is also sufficient to supply the input voltage to the three low power non-isolated POL converters that provide the 1.8, 1.5 and 1.2 volt outputs to the system and are designed to operate from a 3.3V input source. There is usually a power sequencing requirement on multiple voltage systems. A system controller makes the sequencing of the individual POL converters. Since it is desirable to have the 3.3V input bus to the POLs active before individual outputs are turned on, there is also a series MOSFET switch used on the 3.3V output to the system.

In this example a total of four converter blocks are required, 1 isolated and 3 non-isolated. A single conversion stage is used on the 3.3V output while the other three outputs have two conversion stages in series.

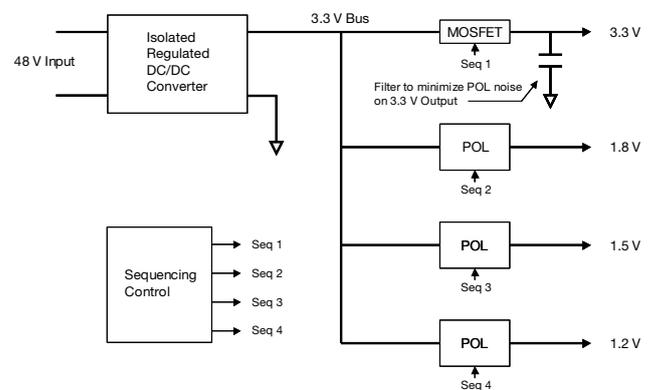


Figure 1

Description of Unregulated Bus Implementation

Description of Unregulated Bus Implementation Figure 2 depicts a system that is implemented with the unregulated bus architecture. As with the previous example, there are four output voltages. However in this case the 3.3V output is not the dominant load, with significant current demands on all of the supply voltages. This system also takes its power from a nominal 48V power bus.

The unregulated bus system employs an isolated but unregulated intermediate bus converter (IBC) function to drop the 48V input

voltage down to a nominal 12 V level for usage by the following POL converters. This voltage reduction is desirable because POL converters operate most efficiently and reliably with a limited ratio between the input and output voltages so that the duty cycle of the buck converter topology can be optimized.

WHILE ADDING A SECOND CONVERSION STAGE MIGHT AT FIRST SEEM UNDESIRABLE, IBC CONVERTERS ARE DESIGNED TO BE BOTH EXTREMELY EFFICIENT AND LOW IN COST.

This is possible because they are unregulated (less complexity and cost) and can operate at a constant 50% duty cycle (higher efficiency). The IBC output voltage is constrained to a fixed value as determined by the turns ratio of the IBC transformer. The IBC therefore can be considered as a “DC transformer”. A 4:1 turns ratio is used in this example to provide the nominal 12 volt output from the IBC. Other commonly used turns ratios are 3:1 and 5:1, resulting in nominal bus voltages of 15 volts and 9 volts respectively. The individual POL converters accomplish the regulation of each of the output voltages.

This system also contains a power sequencing circuit that controls each output by means of the control or enables input to each of the POL converters. Note that the MOSFET used in the regulated bus system is not needed with this architecture nor is the additional filtering on the 3.3V output. In this example, a total of five converter blocks are required, one isolated and 4 non-isolated. Dual conversion stages are used on all four outputs.

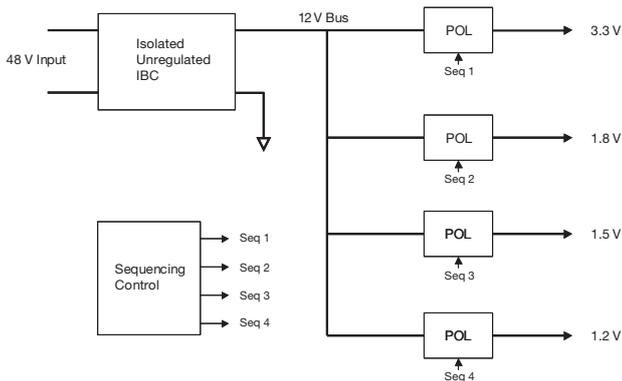


Figure 2

Architectural Selection Considerations

The two architectures described above are both viable in many DPA applications and can each be configured into reliable and

cost effective power systems. Consequently the choice between the two can be difficult at times. Some of the factors that can influence the decision in one direction or the other are described below.

Output Power Level

Systems with a high total output power tend to favor the unregulated bus architecture, especially if high current or power levels are present on two or more output voltages. The regulated bus approach is often the best choice for lower power systems with most of the output power concentrated on one output voltage.

Output Voltages

Systems with a high number of output voltages tend to favor the unregulated bus architecture, since the additional cost and footprint of the IBC module can be amortized over a larger number of outputs. In a system with 3 output voltages, for example, the regulated bus architecture would employ a total of 3 converter modules while the unregulated bus architecture would require a total of 4, a 33% increase. In a system with 6 output voltages, the number of converter modules would be 6 and 7 for the two architectures, an increase of only 16% in the number of conversion elements.

The regulated bus approach tends to work best when the output voltage with the highest current is at a voltage level commonly used as an input for POL converters, such as 5V or 3.3V. If the maximum output power were required at a voltage of 2.5V or lower, the regulated bus architecture would not be a good choice. It also is best when only this one output voltage requires high power or current and the remaining output voltages are ancillary in nature, each requiring a modest amount of power from the DC/DC converter. These lower power outputs are sometimes referred to as “spot power”. If two or more outputs require large or nearly equal amounts of output power or current, the unregulated bus architecture will be attractive and prevent possible problems with interaction between converters that could occur with a regulated bus architecture.

Efficiency

Efficiency is one of the most critical parameters of a power system and it will be a key factor in deciding between the two architectures being considered here. The good news is that both architectures can deliver a highly efficient system. At first glance it would seem that the usage of two conversion stages in series for all output voltages would put the unregulated bus approach at a disadvantage. In practice, however, the unregulated bus architecture can deliver highly efficient systems because of

the very high efficiency of the unregulated IBC, and is typically more efficient than the regulated bus approach for high power systems. To demonstrate this, consider the example shown in Figure 3.

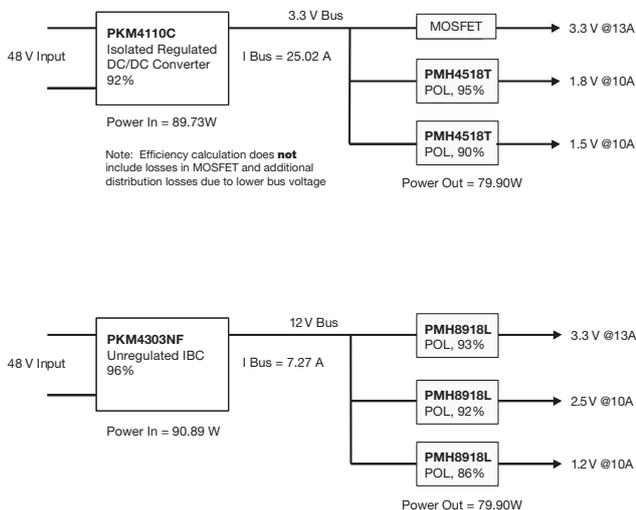


Figure 3

For purposes of comparison the same three output power system is implemented with both the regulated bus and unregulated bus architectures using actual power conversion products available from Ericsson. The specified typical efficiency of each conversion module at the power used in the example is shown in each block in the diagrams. The total output and input power is also calculated along with the overall power system efficiency. The regulated bus system has an overall efficiency of 89.0% while the unregulated bus system has a slightly lower overall efficiency of 87.9%. Note that the loss in the series MOSFET used in the regulated bus system is not included in this calculation. Also note the large difference between the bus currents in the two architectures – 7.3 A for the unregulated bus vs. 25 A for the regulated bus. This is due to the higher (12 V) bus voltage in the unregulated bus solution. The additional bus current in the regulated bus system will result in significantly larger PWB distribution traces and/or larger distribution power losses. If these losses, in conjunction with the MOSFET losses, are 1.2 W or more they will offset the slight efficiency advantage calculated for the regulated bus system in the example. Note that this example is a fairly low power system. The efficiency advantage for the unregulated bus approach will tend to be greater for higher power systems.

The net result for our example is that either approach will be approximately equal in overall efficiency. This is possible because of the very high 96% efficiency of the unregulated IBC. This low cost converter also has very high power density to minimize the space needed on the PWB.

This example also depicts one of the efficiency tradeoffs inherent in selecting the bus voltage. In general, POL buck converters will be more efficient if the ratio between input and output voltage is minimized. This would suggest a low bus voltage such as 3.3 or 5 V. However, the lower bus voltage results in higher distribution losses and more cumbersome distribution design as well as lower efficiency for the intermediate bus converter. The best overall balance and system efficiency is often achieved with bus voltages between 8 and 15 volts. The availability of standardized power modules will also influence this decision.

Thermal Management

Thermal management issues sometimes will influence the selection of a power architecture. While the efficiency and total power dissipation of both of the architectures being explored here are good, there can be subtle differences from a packaging point-of-view. The unregulated bus approach divides the total dissipated power over a larger number of circuit elements and consequently over a more distributed area of the PWB. The placement of each converter module with respect to the system airflow pattern should also be considered. While it is important to place the POL converters close to the load to optimize the dynamic performance and distribution losses, it sometimes is better to place the intermediate bus converter some distance from the POL:s to achieve better distribution of the power losses on the PWB. This can result in lower operating temperatures and enhanced reliability.

External Components

Power converters aren't the only components in a power system, and the number of other components will vary as a function of the architecture selected. For example we have seen that the regulated bus approach will usually require a MOSFET switch for sequencing the main power output of the DC/DC converter. In such systems some type of filter is also needed to prevent the noise on the inputs of the POL:s from interfering with the main DC/DC converter output voltage to the load. The number, type, footprint and cost of decoupling capacitors should also be considered. A typical system requires dozens of them and the requirement will vary with the power architecture selected as well as the design of the individual converter elements. A higher bus voltage will usually result in fewer and smaller capacitors on the bus, as the volumetric energy storage efficiency of capacitors is much better at higher voltages. The functionality integrated into the intermediate bus converters and POL converters should also be considered when making a selection. Not all converters are the same, and some will require additional components to be added for functions such as voltage programming, sequencing and control.

Input Voltage Range

The nature of the 48V input voltage source could often influence the architectural decision. If the voltage swing on the 48V input extends over the full central office telecom range (36 to 75V), unregulated bus architecture will have the same percentage swing on the intermediate bus (9 to 18.7V for a nominal 12V bus). This range is broader than the specified input range on most 12V input POL converters. Consequently this would not be an acceptable approach. Alternatives include using a regulated bus converter, very wide input voltage range POL converters or an alternative architecture.

Many modern telecom and datacom systems utilize 48V input power sources that exhibit a much more narrow range of voltage variation than a conventional telecom system, ie battery systems. These systems are good candidates for the unregulated bus architecture. The PKM intermediate bus converter shown in Figure 3b, for example, is specified to operate over an input voltage range of 42 to 53V with a resulting output voltage range of 10.5 to 13.25V. This output voltage range is consistent with the input voltage requirements of the PMH8918 POL converters. If the POL being considered requires a very tight input range (a regulated input voltage), then the regulated bus approach would be appropriate.

Conclusion

Both the regulated bus and the unregulated bus architectures are useful for the implementation of efficient, reliable and cost effective power systems. Some of the tradeoffs that will help determine the optimal choice for a given application have been discussed in this application note. The table in Figure 4 summarizes the main characteristics of the two architectures. The information in this application note should provide a good general reference to help the power system designer understand the available architectural choices and to make a preliminary selection between them. Ericsson manufactures a wide variety of highly efficient power modules that will support both of the architectures described. These products are supported by extensive detailed datasheets, design notes and application notes that are available from the Ericsson Power Modules website. By using the information from the website it is easy to do preliminary design comparisons between the two architectures. Overall efficiency, PWB board footprint requirements, external components and cost can be compared so that a final architecture can be selected as well as the individual converters to be used for its implementation.

Parameter	Regulated Bus	Unregulated Bus
Efficiency	Low Power System	About Equal
	High Power System	Lower
External Components	MOSFET, Noise Filtering, Load Decoupling Caps	Load Decoupling Caps
Capacitors on Intermediate Bus	More	Less
Total Number and Footprint of Converters	Less	More
Distribution Copper	More	Less
Input Voltage Range	Full Telecom, Datacom	Restricted Telecom, Datacom
Cost	Low Power System	Higher
	High Power System	Lower

Figure 4 - Comparison of two Architectures

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Formed in the late seventies, Ericsson Power Modules is a division of Ericsson AB that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage regulators such as point-of-load units ranging in output power from 1 W to 700 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

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