ericsson.com

# DIGITAL CONTROL TECHNIQUES ENABLING POWER DENSITY IMPROVEMENTS AND POWER MANAGEMENT CAPABILITIES

TECHNICAL PAPER 004
First presented at PCIM China 2007

ERICSSON

Digital control can be used as an enabling technology to offer performance, value, reliability and power density improvements to the end user. A system power management interface may also be added to a BMPS without compromising cost or packaging density.

## CONTENTS


| | | |
|---|---|---|
| | ABSTRACT | 2 |
| 1.0 | INTRODUCTION | 3 |
| 2.0 | CASE STUDY DESIGNS | 3 |
| 2.1 | EXISTING 18 A ANALOG PRODUCT | 3 |
| 2.2 | SIZE-OPTIMIZED 20 A DIGITAL | 3 |
| 2.3 | OUTPUT-OPTIMIZED 40 A DIGITAL | 4 |
| 3.0 | PERFORMANCE COMPARISON | 5 |
| 3.1 | EFFICIENCY | 5 |
| 3.2 | PACKAGING DENSITY | 6 |
| 3.3 | COMPONENT COUNT | 6 |
| 3.4 | COST | 6 |
| 3.5 | RELIABILITY | 6 |
| 4.0 | CONCLUSIONS | 7 |
| 5.0 | REFERENCES | 7 |


### ABOUT THIS PAPER


Material contained in this document has been presented first in March 22, 2007 at PCIM China, session 3 – Future DC/DC Converter Concepts – Part I.


PCIM China is an independent event within Electronica & Productronica China, organized by Munich Exhibitions. Like PCIM Europe, which takes place annually in Nuremberg in Germany, the PCIM event in China is an international meeting ground for specialists in power electronics and its applications in drive technologies and power quality. The event offers a chance to see the latest developments in power electronics components and systems.

## ABSTRACT


This paper presents a detailed analysis of how digital techniques compare with traditional analog approaches in a Board Mounted Power Supply (BMPS). The analysis is based on a case study of a product from an actual production batch. It is shown that replacing some of the analog content with digital circuitry can provide performance benefits to the end user without incurring any penalties in the form of additional cost or design complexity. Power density, in particular, is significantly improved. In addition, work is presented showing how a simple cost effective communication interface can be added to the basic design so that the additional functionality of digital power management can be made available.

## 1. INTRODUCTION

Digital techniques can be applied at several points within a power system, both internal to power supplies and at the system level for purposes of implementing management and monitoring functions [4]. This paper elaborates on the former situation. It compares the effects at the system level of implementation of control functions internal to a Board Mounted Power Supply (BMPS) with digital techniques vs. the more traditional analog approaches. With either of the approaches considered in this comparison, the end user of the BMPS may treat the device in a traditional way without any need for digital techniques at the system level. The comparison is done by means of a case study using an actual production unit as a baseline design. Two digital designs are used in the study. One is a size-optimized design that offers a power output comparable to the analog product but with smaller physical dimensions. The second output-optimized design maintains a form factor similar to the analog version but increases the power output. The basic power train topologies remain constant across all three versions so that the focus of the comparison is the design flexibility made available due to the utilization of digital control techniques.
Some of the areas of interest in the comparison are electrical performance and efficiency, parts count, power density, cost and reliability. The comparison is done from an end-user's perspective rather than focusing on benefits to the BMPS designer.

The BMPS used in the case study comparison is an Ericsson PMH8918L Point of Load (POL) regulator [1]. This is an 18 amp non-isolated synchronous buck regulator with a programmable output voltage and a nominal 12 V input voltage. This is a recent product with competitive specifications, so it is a good representation of a POL regulator using analog control. A previously published paper [3], estimated that digital techniques could reduce the required Printed-Circuit-Board (PCB) area by 40 to 50% for the same 18 A output current or allow an output current of 35 A in the same package size. This paper will show that these estimates were in fact too conservative and that even higher power and current densities are possible when using digital control techniques.

In addition to considering the user benefits of the digital control design internal to the POL regulator, a new interface connector was added to the digital versions so that digital power management techniques could optionally be used in the power system. The addition of this connector does not change the measured performance of the POL regulator or the results of the comparison between analog and digital control methodologies. The connector addition was done to demonstrate that providing this optional system capability could be accomplished without substantive negative impact on the cost or size of the BMPS.

The content of this paper is limited to the technical and performance trade-offs at the BMPS level as described above. To provide a broader context, including extension of digital techniques into the arena of power system management, the reader is directed to the white paper in reference [4].

## 2. CASE STUDY DESIGNS

### 2.1 EXISTING 18 A ANALOG PRODUCT

The Ericsson PMH8918L Point of Load (POL) regulator has a nominal output current of 18 A. It uses a non-isolated synchronous buck topology with a traditional analog control loop and operates at a switching frequency of 320 kHz. The output voltage is programmable between 1.2 and 5.5 V and the input voltage is nominally 12 V. The typical efficiency at 3.3 V output is over 92% and the calculated MTBF is 3.8 million hours.

The upper MOSFET has an $R_{DS\text{-}ON}$ specification of 8.8 mΩ and a gate charge specification, Qg, of 11 nC. The corresponding values for the lower MOSFET are 4.0 mΩ and 27 nC. The output inductor has a nominal value of 1.2 µH and a resistance of 2.3 mΩ.

The dimensions of the PMH8918L POL regulator are 38.1 x 22.1 x 9.0 mm. A photograph of the through hole version is shown in *Figure 1*.

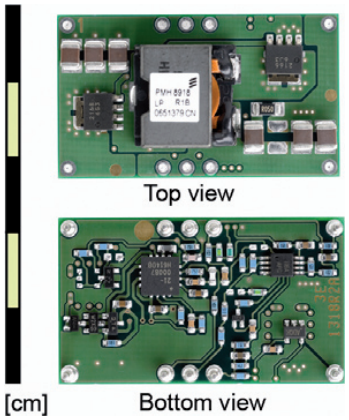


Figure 1 – PMH8918L analog design

### 2.2 SIZE-OPTIMIZED 20 A DIGITAL

A digitally controlled POL regulator was constructed that was capable of approximately the same output current and power as the analog PMH8918L. The basic topology was the same. A new PCB layout was used in order to optimize the size. The dimensions of the finished POL regulator were 25.4 x 12.7 x 8.5 mm and it was capable of supplying a maximum output current of 20 A.

It is important to be aware that much of the size reduction that became possible in this design was due to the lower component count associated with the digital control implementation. The higher level of integration eliminated several discrete housekeeping components used in the analog design. The efficiency was optimized by careful selection of the MOSFET devices and by minimizing the sum of MOSFET switching losses and conduction losses. The upper FET has an $R_{DS\text{-}ON}$ of 3.4 mΩ and a Qg of 30 nC. The lower FET has values of 1.8 mΩ and 47 nC. The lower RDS-ON values in combination with lower source inductance of the new devices result in a lower total for combined conduction

and switching losses and optimize efficiency at full load. The output inductor is 1.0 µH with a resistance of 2.3 mΩ. The amount of copper in the PCB was also changed to allow for improved thermal management and minimized conduction losses.

The control chip used in this design features an "efficiency optimized dead time control". This feature results in enhanced efficiency as will be demonstrated later in this paper. More information about this technique can be found in reference [2]. This POL regulator operates at a switching frequency of 320 kHz.

Although they do not affect the performance of the designs and are not needed for basic functionality, a new signal interface connector was added to the digitally controlled POL regulators in this case study. Rather than using high current pins suitable for power connections, a simple standardized cost-effective 10 pin connector was designed. If desired by the end user, this connector can be used for purposes of communicating with system level power management circuitry and configuration of the POL regulator. By including the connector in these designs, it can be shown that it will not adversely affect the package size. A photograph of the completed 20 A size-optimized digital design is shown in *Figure 2*.

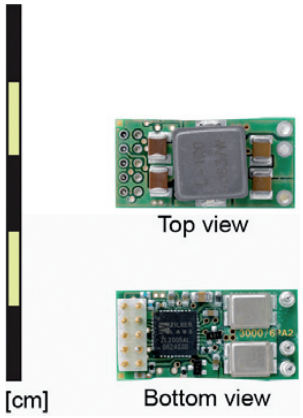


Figure 2 – Size-optimized digital design

### 2.3 OUTPUT-OPTIMIZED 40 A DIGITAL

Another digitally controlled POL regulator was constructed in a size similar to that of the analog PMH8918L but with enhanced output current capability. The final size was slightly less than the analog version, with final dimensions of 30.0 x 20.0 x 8.5 mm. The output current capability of this POL regulator was 40 A.

In order to support the higher current level, parallel MOSFETs are used in this design. The FET devices were selected based on the same criteria as the size-optimized design. The upper FETs have a combined RDS-ON of 1.7 mΩ and Qg of 60 nC. The lower devices' combined values are 0.6 mΩ and 141 nC. The inductor is 0.82 µH with a resistance of 1.7 mΩ to further minimizing the resistive losses. This design also operates at a frequency of 320 kHz using the same control chip as the 20 A digital design.

A photograph of the 40 A output-optimized design is shown in *Figure 3*.

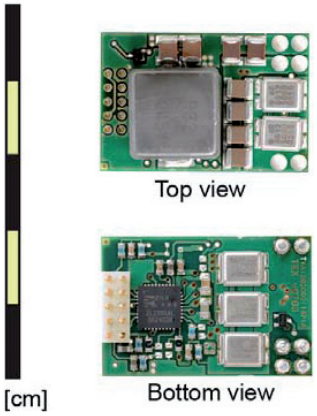


Figure 3 – Output-optimized digital design

## 3. PERFORMANCE COMPARISON

The three designs used in this case study are being characterized in terms of the normally accepted electrical performance parameters. These include output line and load regulation, efficiency, ripple and noise, and dynamic response. Due to the space limitations of this paper, we will only discuss efficiency in detail since it is a critical parameter that is of high importance to the end user. We can summarize the other electrical parameters identified above by saying that in all cases the performance of the two digital designs are equal to or better than the analog baseline design. Some of the preliminary comparative data can be found in reference [3].

### 3.1 EFFICIENCY

The PMH8918L used in this design comparison is a high current POL regulator. For this type of product, conversion efficiency is extremely important as it has a large influence on the system thermal design and ultimate packaging density as well as determining the input power required by the end equipment. Consequently, if digital control techniques compromise the efficiency they would not be an acceptable approach.

Curves showing the efficiency vs. output current for the three designs used in this study are shown in *Figures 4, 5 and 6*. The data for each of these curves was taken with an input voltage of 12 V, an output voltage of 3.3 V, and at an ambient temperature of +25°C. Comparing the 20 A digital design with the 18 A analog design shows that the digital implementation resulted in an efficiency improvement across the entire load range in spite of the significantly smaller size of the digital module. At half load, the digital POL regulator was 1.1% more efficient (93.8%) and at full load it was 1.2% more efficient (92.5%). The efficiency improvement in the digital design is achieved thanks to elimination of house-keeping circuitry and the dead-time control, but also thanks to a more optimized power-train.

Because the baseline analog POL regulator is designed and characterized at 12 V input, we used this input voltage to get comparable data for the digital design. As a side note, the efficiency of the digital design is even higher at lower input voltages. For example, its efficiency is approximately 1% better (94.8%) at half load when operated at an input voltage of 9.6 V. This could be an interesting area to explore for purposes of optimization of overall power system efficiency.

The 40 A digital design was optimized for higher current, and this is reflected in its efficiency performance between 15 and 30 A as shown in *Figure 6*. At under 10 A output, which includes much of the useful operating range of the 18 A analog design, its efficiency will be somewhat less than that of the analog POL regulator duo to higher switching losses. Its efficiency at half load (20 A) is 93.7% which is a 2.4% improvement over the efficiency of the analog design at a comparable current. At a full load output of 40 A, the efficiency is 91.9%, which is still 0.6% better than the analog POL regulator at full load. So over its intended design range, the 40 A digital also outperforms the analog design in terms of efficiency. The improvement can be attributed to the same elements as with the 20 A design. The 40 A design is also up to 1% more efficient when operated at 9.6 V input.

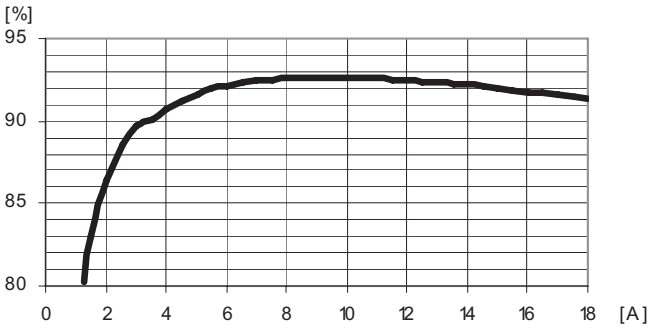


Figure 4 – Analog design Efficiency, Vout=3.3 V, T=25°C

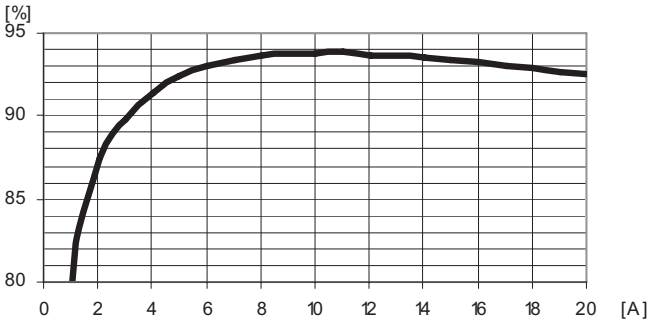


Figure 5 – 20 A Digital design Efficiency, Vout=3.3 V, T=25°C

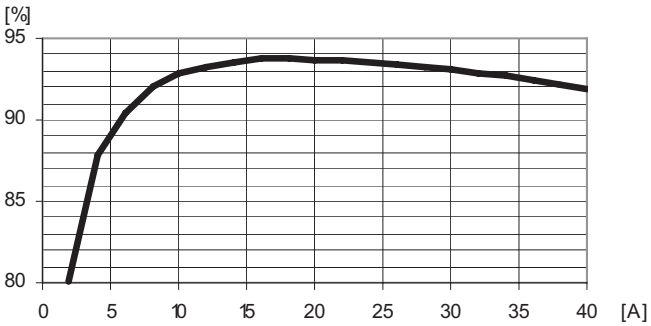


Figure 6 – 40 A Digital design Efficiency, Vout=3.3 V, T=25°C

Even though the 40 A digital design is more efficient than the analog POL regulator and is approximately similar in size, it will have a larger power dissipation because it is capable of over twice the output power and current. This results in a larger power density in terms of heat that needs to be removed from the BMPS. While the previous analog designs were size limited by the component packaging density, this type of digital design could be size limited by the heat transfer mechanisms for cooling the BMPS. That is, if conventional packaging materials and cooling paths are used, generating 40 A from a BMPS of this size could require additional attention to thermal management and ambient temperatures in the end-user's equipment.

### 3.2 PACKAGING DENSITY

Packaging density is heavily influenced by efficiency and is equally important to the end user. The reduction in component count in the digital designs, to be discussed below, contributes significantly to the higher packaging densities obtained. We have calculated density in two ways. The first is area current density expressed in terms of output amps per $cm^2$ of board area used by the POL regulator. The second is traditional power density calculated from the POL regulator maximum output power at 3.3 V and expressed in terms of watts per $cm^3$.

The 20 A digital POL regulator has a 289% better area current density and a 307% better power density than the baseline analog design. The 40 A digital POL regulator has a 312% better area current density and a 330% better power density than the baseline analog design. Stated another way, the 20 A digital design provides an additional 2 A of output current along with a reduction of 61% in board area vs. the analog product. The 40 A design provides a 22 A (122%) increase in current with a board area reduction of 28% compared to the analog design.

### 3.3 COMPONENT COUNT

The baseline POL regulator design using analog control used a total of 58 components excluding connector pins but including the PCB as one component. Using the same ground rules, the 20 A digital design has 24 components and the 40 A digital design has 41 components. As noted previously, this major reduction in parts was primarily responsible for the enhanced power densities achievable with the digital designs. In addition to the packaging improvements, the reduced parts count is expected to play a major positive role in the cost and reliability of future designs using digital control.

### 3.4 COST

Since PMH8918L is a production unit, the cost structure of the analog design is known with a high degree of accuracy. The digital designs are in prototype form and utilize some components, such as the digital control chip, that have been quite recently introduced and consequently do not have a well established pricing history. Furthermore, we expect that as digital control techniques receive wider acceptance the prices for some of the specialized components will decline. We therefore do not present a detailed cost analysis here. But because of the much higher degree of integration shown to be possible with digital techniques, along with their higher level of electrical and packaging performance, we are convinced that digital solutions will soon provide a much higher level of value to most users.

### 3.5 RELIABILITY

Detailed reliability calculations have not as yet been done for the prototype digital designs. The 18 A analog design has a calculated MTBF of 3.8 million hours. The two digital designs were done with the same component derating practices as used in the analog version. The lower parts count should more than offset the higher current levels in some areas of the digital designs. In general, the high degree of integration and fewer component interconnections of the digital designs should bode well for their reliability.

## 4. CONCLUSIONS

As a result of this case study several conclusions can be made about the viability of digital control in POL regulators relative to analog designs:

- THE GENERAL ELECTRICAL PERFORMANCE OF THE DIGITALLY CONTROLLED REGULATORS IS EQUAL TO OR BETTER THAN THE ANALOG VERSION.
- AT THE SAME CURRENT LEVEL, THE EFFICIENCY OF THE DIGITAL DESIGNS IS HIGHER THAN THAT OF THE ANALOG VERSION. EFFICIENCY IMPROVEMENTS IN EXCESS OF 1% ARE POSSIBLE.
- THE DIGITAL DESIGNS HAVE A DEFINITE ADVANTAGE IN TERMS OF PACKAGING DENSITY. THIS CAN BE USED TO MAKE BMPS SMALLER OR TO INCREASE THE POWER AVAILABLE WITHIN A STANDARDIZED PACKAGE SIZE.
- THE DIGITAL DESIGNS EXHIBIT DRASTICALLY IMPROVED CURRENT AND POWER DENSITIES WHEN COMPARED TO THE ANALOG POL REGULATOR, RANGING FROM 289% TO 330%.
- WITH THE INCREASED INTEGRATION OF THE 40 A DIGITAL DESIGN, THE PACKAGING LIMITATION BECOMES HEAT REMOVAL RATHER THAN COMPONENT AREA.
- THE DIGITAL DESIGNS SUBSTANTIALLY REDUCE THE PARTS COUNT, A 58% REDUCTION FOR THE 20 A DESIGN AND 29% FOR THE 40 A VERSION.
- ALTHOUGH DETAILED COST ANALYSIS IS NOT YET VIABLE, DIGITAL DESIGNS ARE EXPECTED TO OFFER OUTSTANDING VALUE TO THE USER WHEN COMPARED TO ANALOG BMPS.
- DUE TO LOW PARTS COUNT AND INCREASED INTEGRATION DIGITAL DESIGNS SHOULD PROVE TO BE EVEN MORE RELIABLE THAN ANALOG IMPLEMENTATIONS WHEN PREDICTIVE MTBF CALCULATIONS ARE USED.

In conclusion, digital control can be used as an enabling technology to offer performance, value, reliability and power density improvements to the end user with no additional design effort required from the OEM system designer. If desired, a system power management interface may be added to BMPS without compromising cost or packaging density.

## 5. REFERENCES


[1] Ericsson Power Modules: PMH8918L Technical Specification, April 2006, www.ericsson.com

[2] Zilker Labs, Inc.: ZL2005 Datasheet, 2006, www.zilkerlabs.com

[3] Ericsson Power Modules: “Performance Improvements for OEM System Designers – a Digital Control Case Study”, September, 2006, www.ericsson.com

[4] Ericsson AB: “Power supply goes digital”, October 2006, www.ericsson.com


All referenced papers and data sheets can be found at Ericsson Power Modules’ web site: http://www.ericsson.com/powermodules


10/287 01-FGB 101 378 Uen Rev B 2010-06-30